Design Automation of Integrated Circuits by Network-on-Chip Technology

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Abstract – **Network-on-chip (NoC) is a new paradigm for interconnection within IC. The NoC design automation is the actual task providing the effective implementation of complex electronics devices. The automated design algorithm and description of program for NoC implementation are given.**

Keywords –**Network-on-Chip, CAD, automated design.**

I. INTRODUCTION

Currently, integrated circuits are used in a wide range of areas. Buses and point to point connections are the main means to connect the components. Buses can efficiently connect 3-10 communication partners but they do not scale to higher numbers. Even worse, they behave very unpredictably as seen from an individual component, because many other components also use them [1]. To solve these problems in a chip the Network-on-Chip approach was proposed. It provides the communication infrastructure for connecting components into a single system. Because of the complexity of such systems, it cannot be designed without automation.

II. AUTOMATED DESIGN ALGORITHM

There are four main tasks that must be solved when designing a communication infrastructure of NoC-system:

- topology selection;
- switch type selection;
- routing algorithm selection;
- resource allocation.

To solve these tasks the next automated design algorithm was formulated:

1. Creating a component models library.
2. Forming the input description of the system.
3. Creating different communication structures by the library models corresponding to the input description.
4. Modeling and best solution selection.
5. Creating a description of the selected solution in one of the HDL-languages (VHDL, Verilog).

III. PRACTICAL IMPLEMENTATION

Described algorithm was implemented as a CAD-subsystem. Component models for all levels of design were created: object models for working in automation program, Simulink-models for transaction level verification in MATLAB, VHDL-models for RTL level verification in ModelSim and synthesis in Xilinx ISE. Models of resource and switches for Mesh and Tree topologies were created.

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Input description of system is a list of links between components and required performance for them.

The resource allocation algorithms were developed and implemented for creating different communication structures.

The quality of the solution is evaluated as maximum required link performance. Required link performance is calculated using the following formula:

$$perf = Constr_i \times (N_{Links} + 1) \times SwDelay\ , \qquad (1)$$

where $Constr_i$ - constraint for the *i*-th link from the input description, N_{Links} - number of links between resources in topology, $N_{Links} + 1$ - number of switches between resources in topology, $SwDelay$ - delay of the switch.

As an experiment automated design of video processing systems, such as MPEG4-Decoder [3], VOP (Video Object Plane)-decoder and PiP (Picture-in-Picture) device [2], was done.

Experiments have shown that Mesh topology is much more effective for VOP-decoder but is more expensive, and Tree topology slightly more effective for other two devices and requires fewer switches and links. These results confirm the theoretical conclusions about the applicability of the topologies and therefore it can be said that the developed program is working correctly.

IV. CONCLUSION

Network-on-Chip is rapidly evolving technology and it's automatization is actual problem. In this paper the computer aided design algorithm and results of experiments with the program that implements this algorithm are given. Developed program can be improved by expanding models library, optimizing internal algorithms and adding estimates of the area and power consumption.

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