Як видно з рис. 1 і рис. 2 джоулеві тепловиділення $Q^{(1)}$ складаються з послідовності теплових імпульсів, промодульованих функцією $\varphi^2(t)$, пондеромоторна сила $F_z^{(1)}$ є стискаючою і має осцилюючий в часі характер. Зміна в часі температури пластини (рис. 3), внаслідок дії радіоімпульсів, має характер теплового удару зі скінченною швидкістю.

На рис. 4 показано зміну в часі нормальних до лицевих поверхонь пластини напружень $\sigma_{zz}{}^F$, зумовлених дією пондеромоторної сили (рис. 4, а), і $\sigma_{zz}{}^T$, зумовлених джоулевим нагрівом (рис. 4, б). Звідси видно, що нормальні напруження в пластині при дії радіоімпульсів повністю визначаються дією пондеромоторної сили. На рис. 5, а і 5, б, відповідно, зображено зміну в часі тангенціальних напружень $\sigma_{xx}{}^T$ (рис. 5, а) і $\sigma_{xx}{}^T$ в пластині, зумовлених дією радіоімпульсів. Як видно з рисунків, тангенціальні напруження $\sigma_{xx}{}^F$ і $\sigma_{xx}{}^T$ є однакового порядку з нормальними напруженнями $\sigma_{zz}{}^F$.

Висновки

На основі проведеного числового аналізу можна зробити висновок, що термонапружений стан електропровідної пластини, що перебуває під дією квазіусталених радіоімпульсів на поверхнях, визначається як дією пондеромотрої сили, так і джоулевим нагрівом. Результати числового аналізу узгоджуються з дослідженнями, проведеними для порожнистого циліндра при дії квазіусталених радіоімпульсів [5].

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SOI-MOSFET'S BODY POTENTIAL: FLOATING OR FIXED?

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Розглянуто сучасні технології в електронній промисловості, на зразок SOI.

Relatively new and more and more advanced technologies like SOI although commonly applied, still remain promising, developing and conceal some ambiguous phenomena.

Introduction

Continuous technology development results in instant technology improvements and changes. Electronic industry demands higher operating frequencies, reduced power and increased circuits complexity. Therefore more and more advanced structures are designed to fulfill market expectations and meet commercial profits. Along with the technology evolution, more and more subtle phenomena can no longer be neglected. Some of them, absolutely insignificant in the past, now become important. Hence, modeling capability extension is a must.

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Nomenclature

W	– channel width	[cm]
L	– channel length	[cm]
μ_0	– effective carriers mobility in the channel	[$^{cm2}/_{V \cdot s}$]
ε_{Si}	– semiconductor permittivity	[$^{F}/_{cm}$]
U_T	– threshold voltage	[V]
φ_F	– Fermi potential	[V]
φ_{msi}	– metal – semiconductor exit work difference	[V]
q	– electron charge	[C]
Q_{eff}	– surface traps' effective charge density	[$^{C}/_{cm^2}$]
Q_C	– channel mobile charge density	[$^{C}/_{cm^2}$]
C_i	– gate oxide capacitance density	[$^{F}/_{cm^2}$]
N	– effective doping of the substrate	[$^{1}/_{cm^3}$]
v_{SAT}	– carriers saturation mobility	[$^{cm}/_{s}$]
E	– electric field	[$^{V}/_{cm}$]
E_L	– lateral electric field in the channel	[$^{V}/_{cm}$]
β	– empirical fitting parameter. Usually ranges between 1.4 – 1.5	
s	– body semiconductor type's selector: $s = \frac{\varphi_F}{\lvert\varphi_F\rvert}$	[-]
U_{SB}	– source – body voltage	[V]
U_T	– threshold voltage	[V]

Mos channel operating rules

There are two mainstreams in contemporary microelectronics: devices based on traditional BULK substrates, and more advanced - developed on SOI ones.

Experimental data [5] show that PD SOI MOSFET device has 20-30% performance improvement over its BULK counterpart. This improvement comes from reduced junction capacitance area (for approx. 45%), from lower threshold voltages (for approx. 45%) and from other – less important factors (for approx. 10%).

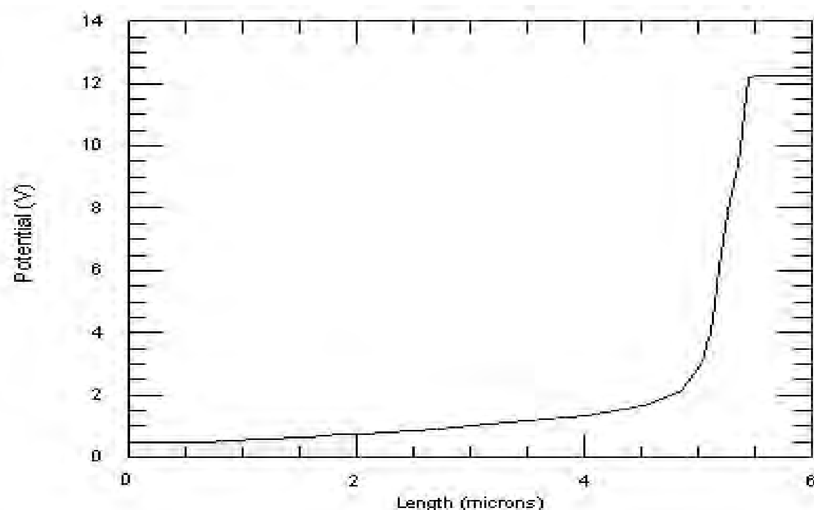

Fig. 1. SOI versus BULK's substrate based device structure

Let us have a look at main difference between bodies used in microelectronics industry. BULK devices are developed on a single part of substrate (or well). Hence, if there is no additional insulation,

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their bodies are not electrically separated. SOI substrates in natural way offer almost ideal electrical device-to-device insulation. No additional implantation, diffusion nor annealing is necessary. Simple local substrate's anisotropic etching perfectly separates devices. Very important is also the fact, that insulation in SOI is considerably less silicon area consuming technology than conventional BULK one. Excellent insulation also enables SOI devices for operating in radiation -hazardous environments.

MOS devices can work in three modes of operation [2]:

- cut-off - when there is no channel induced (opened) and approximately no current flows between the source and drain
- active - when the channel is induced (opened) at a full distance between source and drain. The drain current follows the gate voltage
- saturation - when the external polarization of the drain is strong enough that the channel exists not in a full length between source and drain. It means that there is an area almost completely depleted [9] of minor carriers near the drain.

Let us consider for the rest of this article only the BULK- and SOI - NMOSFET transistors.

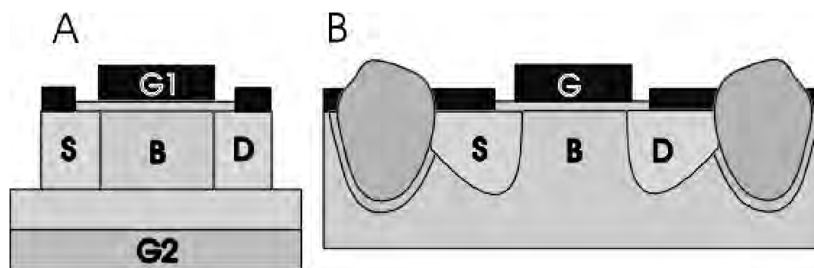

Fig. 2. SOI ⇔ BULK's substrate based device structure

What is going with electrons – the bulk minority carriers - in the induced channel? At the beginning of the channel, close to the source, electrons start their trip to the drain at the minimum velocity. The channel is in strong inversion, which comes from the orthogonal electric field component generated by the gate. It is strongest in the source end of the channel. Therefore the channel is thick, and many relatively slow electrons compose the drain current. As we slide in to the drain direction, electrons speed-up with the lateral electric field's component, when the orthogonal component value decreases. Now simultaneously: the channel becomes thinner, the lateral components of the channel electric field – amplify, and - according to Eq.1 - the average mobility of electrons' saturates.

$$\mu(E_L) = \mu_0 \frac{1}{\sqrt[\beta]{1 + \left(\frac{\mu_0 E_L}{v_{SAT}}\right)^{\beta}}} \tag{1}$$

Above described phenomena reduce the local surface charge density of the channel electrons. As the total drain current for the given external transistor's polarization is constant, also the current flow in each orthogonal cross section along the channel must stay unchanged. It is because there are maintained many of balances in MOS transistor. Some – the most important of them – are:

- limit of the surface charge density of the drain around the orthogonal cross section of the channel,
- thinning of the channel depth,
- increase and saturation of the carriers velocity,
- linear increase of the channel's lateral electric field

When the carriers' velocity saturates (achieves maximum value) the physical properties of the channel change. When velocity is the highest possible one, and as the total drain current value is the same everywhere inside the channel, the point where it happens, is where the channel physically achieves saturation, achieves minimum thickness and where the lateral field achieves its top intensity.

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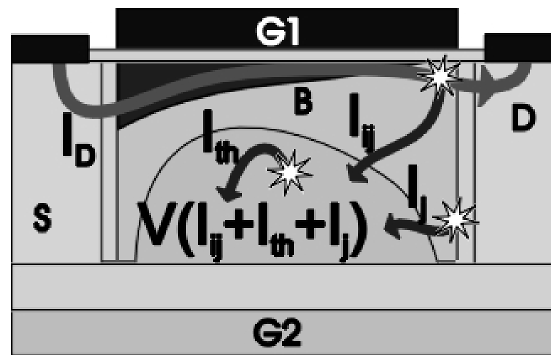

Fig. 3. Soi - body potential modification sources

The voltage drop along the channel (Fig.1) stays unchanged and equal to V_{DSSAT} even when $V_{DS}>V_{DSSAT}$. The entire (V_{DS}-V_{DSSAT}) residual voltage drop spreads over the part of the area between the drain and the active pat of the channel– where the strong inversion condition is yet fulfilled. Length of this– saturated– part of the channel depends on VDS voltage and comes from saturation of the carriers' velocity (here minority carriers in the bulk are the majority carriers in the inverted channel area).

Does floating body really float?

There are several sources (Fig.3) of the mobile charge in the MOS transistors. The mobile charge might come from the thermal generation (I_{th}), from the drain-induced barrier lowering [3] (DIBL effect), from backward polarized bulk-drain junction (I_j). Another source of the charge is the impact ionization (I_{ij}) that occurs in strong electric fields. Such a type of ionization is characteristic for saturated part of the channel. The electric field value ranges $10^5\ ^V/_{cm}$ in this area.

In the BULK (Fig.2b) substrate NMOS devices all the generated positive charge is pushed directly to the body contact which is usually on the lowest potential available in the circuit (in PMOS devices it is negative charge and body is attached to the highest available potential). Finally, the potential of the bulk does not change.

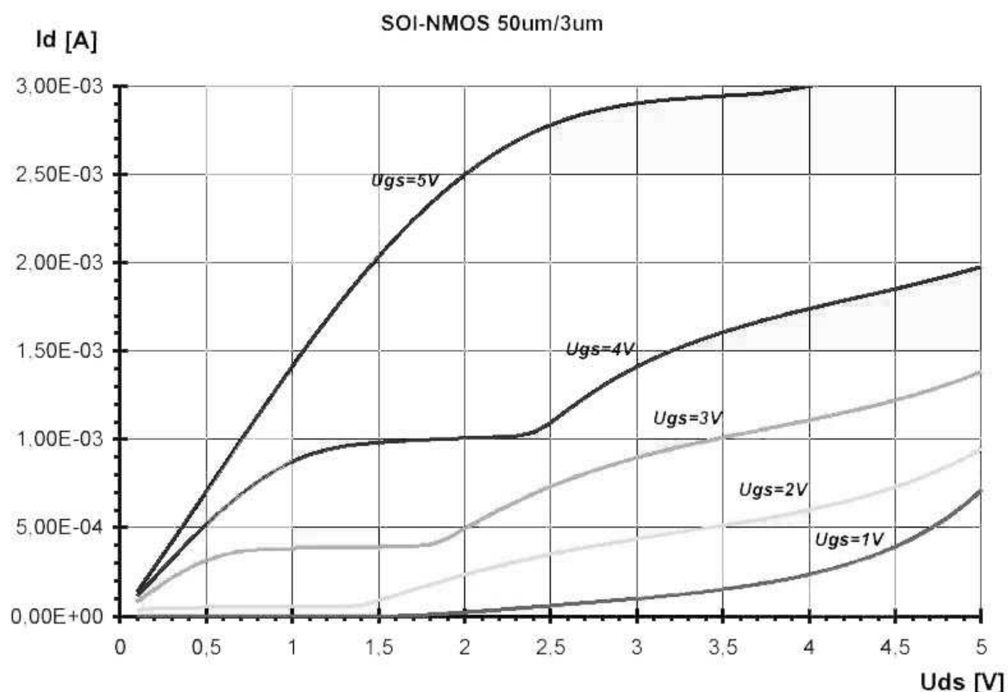

Fig. 4. Kink effect present only in SOI devices

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Electrical insulation between the devices, which are made on SOI substrates (as illustrated on Fig.2a and Fig.3) also separates adequate active silicon areas under the gate. All the charge generated in the device, in contrast to the BULK transistors, accumulates in this area. According to Gauss law and Poisson's equation [1,2], along with the increase of total charge accumulated in the body, its potential changes. Moreover, all of the backward polarized B-D junction minority carriers' current flows through the body to the grounded source. Circuits‘ simulators like SPICE [11] model this phenomenon in much simpler way, usually as two: body-source and body-drain diodes, which are connected in opposite directions and set the body potential. Such an approach neglects many important physical aspects of the MOS transistor's operation. Simulators like STAR-HSPICE for selected SOI device models (for example LEVEL 58) do not support body contact at all.

According to Eq.2 and [1] the changing body potential affects the threshold voltage VT of the MOS transistor.

$$U_T = \varphi_{msi} - \frac{Q_{eff}}{C_i} + \varphi_F + s\frac{\sqrt{2\varepsilon_{Si} qN}}{C_i}\sqrt{\left|2\varphi_F + U_{SB}\right|}. \qquad (2)$$

Well known explanation is as follows: inverted channel area makes virtual junction between bulk (p-type) and n-channel (inverted p-type). For the given gate polarization the orthogonal electric field lines end on yet uninverted, but still depleted part of the channel. Increase of the body potential, reduces the backward polarization of a bulk-channel virtual junction. Finally, depleted area thins-down and more gate orthogonal electric field lines end in the inverted channel area. This causes the increase of the total channel charge and according to the Eq.3 also of the total drain current I_D [1,6].

$$I_D = W\mu_0 Q_C(L)E(L). \qquad (3)$$

It's equivalent to the reduction of the threshold voltage. Nevertheless, there is a limited area of application for the explanation presented above, and for the corresponding algorithms implemented in device/circuits simulators. When the body potential grows up, and finally is close to the drain voltage the MOS transistor should behave – and in really behaves – as an ordinary diode! Models used for simulations do not fit it.

As the total drain current changes, saturation parameters and amounts of generated mobile carriers follow variations of the body potential. Therefore, if the body potential is not fixed by the additional external contact, it is necessary to define and elaborate it precisely. It is especially important in case of SOI devices, where there is no use in attaching the body to any external potential. There is also known a special side effect called "kink effect" in SOI transistors' behavior. It is not observed in BULK devices, but strong and commonly met on PD SOI MOSFET $I_D(U_{DS})$ characteristics (Fig.4). The reason is simple: the SOI-PD structure is sensitive for body potential changes, and range of those changes is significantly wider than in BULK devices. Partial or full depletion of the silicon under the induced channel (transistors PD-SOI and FD-SOI respectively) is also the important factor, because in case of fully depleted devices, the floating body phenomena is very limited.

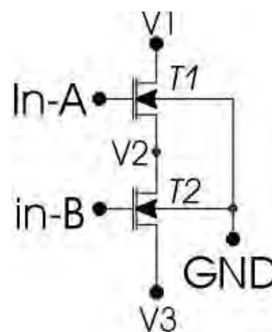

Fig. 5. Effective polarization of the SOI/BULK transistor

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In case of SOI-CMOS gates, leaving the body unconnected is a good solution to omit the differences in effective transistor's gate polarization (U_{GS}). As presented in Fig.5, transistors T1 and T2 work independently when their bodies are not connected nor grounded. If they are connected and/or grounded – the polarization of T1 when T2 is turned-off is less effective (higher $V_{T\,T1}$).

Implemented algorithms

The most popular SOI circuit simulators are based on classic BULK-device oriented algorithms, implemented in basic SPICE engine. It is in case of BSIM-SOI and SOI-SPICE [10, 11] standards. Body potential is a pretty example here. It is iterated in the same way as it was done 10 years ago for several-times bigger devices produced on different substrates.

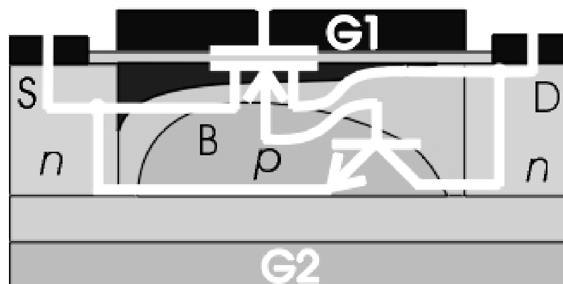

Fig. 6. The main MOS and parasitic bipolar transistors

As time goes on, this approach becomes less accurate. It's necessary to remember that device dimensions are more and more limited and new parasitic devices might enable one day. First among them is the parasitic bipolar body transistor. As it is presented on Fig.5, the semiconductor located between source and drain– in modern MOS devices with the channel length about single nm orders of magnitude– is comparable with the bipolar transistor's base. It is also comparable with the carriers' diffusion free path.

Therefore there is also possible the significant bipolar transistor's action in modern MOS devices, especially those made in SOI technology.

Conclusions

Some ideas, commonly used in the past, now – although they stop working for submicrometer devices – are equipped with additional fitting parameters, and still run. Therefore modern devices require new – more physical and universal models.

Future works

Future works cover extensive experiments with the modeling of bipolar parasitics present in the MOS devices based on both: SOI and BULK substrates. Experiments also will be done on the basis of the BSIM and BSIM-SOI standard models.

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