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Linear mode of single bit high order sigma-delta modulator

Abstract. *There is considered the simulation mathematical model of single bit high order sigma-delta modulator in this paper. It is formulated the condition and criterion of this modulator operation in linear mode.*

Keywords: High Order Sigma-Delta Modulator, Linear Operation Mode, Simulation Model

The sigma-delta modulators (SDM) are the base of most precision analog to digital converters (ADC) at the present time [1, 2]. Usually DSMs are divided to single- or malty- bit according to the capacity of output code [3]. The precision ADC are usually based on single bit SDM [4, 5]. The single bit SDMs are divided to first- second- e.t.c. order according to the number of feedback loops.

The structure of single bit high order SDM is presented on fig. 1. Its forward signal's line consists of the set of summators ⊗, the set of integrators ∫ and synchronous comparator SC, which consists of asynchronous comparator and synchronous D- trigger TT. The feedback loop consists of single bit digital to analog converter DAC controlled by output code of SDM. The trigger TT is synchronized by clock generator G. The most impotent points of the SDM are signed by letters in the circle. The output code of SDM - Nx(t).

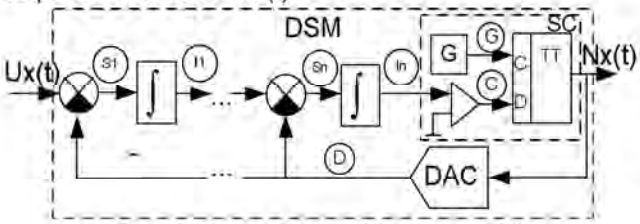

Fig.1. Structure of single bit high order SDM

The investigation of high order SDM [6] detected the problem of SDM operation in linear operating mode for input signals in wide dynamic range. It is caused by the fact if output signal of some integrator exceed feedback signal the next integrator can not discharge. It is because this next integrator continues integration the same polarity signal that it was in the previous cycle. So the direction of moving of output signal of this integrator is not changed and integrator comes to saturation. It breaks the forward signal's line and fixes the output code of DSM. So the main objective of this work is in investigation of conditions of absence the described effect and providing the stable operation of high order SDM.

According to the traditional conception of stability of discrete systems [7] "the limited output signal in the condition of limited input signal" the SDM is always stable because its output signal has limited number of conditions. So the indicated before condition of stability is always true. Therefore in this case it is necessary to consider the condition of SDM's operation in linear mode instead its stability. Linear mode we consider as proportional increasing of output signal to increasing of input signal.

The investigation of simulation model of high order SDM [6] allow us to egest the condition of its operation in linear operating mode. This condition for n-order SDM can be presented as

$$U_{I\,MAX\,i} < E, i = \overline{1, n-1} \quad , \tag{1}$$

where E – output voltage of feedback DAC; $U_{I\,MAX\,i}$ – the maximal allowable output voltage of i-th integrator, which is achieved in the end of integrating loop when the output voltage of previous integrator or input voltage for first integrator is maximal allowable and opposite to the voltage of output voltage of DAC.

As the result of solving the system of equation, which describe the simulation model of SDM, and taking into consideration the condition (1) we get the criterion of the operation in linear mode the arbitrary single bit SDM. This criterion we can present as

$$\sum_{i=1}^{m}\left(\frac{T^{m-i+1}}{(m-i+1)!}\prod_{j=i}^{m}\frac{1}{\tau_j}\right) < E\frac{1-K}{1+K}; m = \overline{1, n-1} \quad ,$$

where $K = U_{X\,MAX}/E$, $U_{X\,MAX}$ - maximal allowable input voltage of linear operation mode of SDM; T – period of clock generator; τ_j – reaction time of appropriate integrator.

The paper is dedicated the investigation of the models of SDM with variable number of order and parameters computed according to the obtained criteria.

Therefore there is done analysis of simulation mathematical model of high order single bit sigma-delta modulator, which allows to formulate the condition and to obtain criterion of operation in linear mode of modulator with arbitrary order and parameters. The simulation of SDM operation confirms the linear mode for input signal variation in the defined limits.

[1] Kester W. Which ADC Architecture Is Right for Your Application? // Analog Dialogue. – 2005. – Vol. 39, № 2. pp.11-19 (URL: http://www.analog.com/library/analogdialogue/archives/39-06/architecture.pdf).

[2] Fowler K. Part 7: analog-to-digital conversion in real-time systems. IEEE Instrumentation & Measurement Magazine. 2003. Vol. 6. Issue 3. pp. 58-64.

[3] Fernando Medeiro, Angel Pérez-Verdú, and Angel Rodríguez-Vázquez. Top-Down Design of High-Performance Sigma-Delta Modulators. (The Springer International Series in Engineering and Computer Science). Kluwer Academic Pub. 1999. p. 287.

[4] Walt Kester. Data Conversion Handbook. ISBN 0750678410. 2004. p. 953.

[5] Golub V.C. Sigma-Delta Modulators and analog to digital converters // Technology and Design in Electronic Devices, 2003, № 4, pp. 35 – 41. (In Russian)

[6] Kochan R.V. Influence of Integrator's Parameters on Nonlinearity of High Order Sigma-Delta Modulator // Acquisition and Processing of Information. 2010, Num. 33(109), pp. 52 – 59. (In Ukrainian)

[7] Kuzin L.T. Computing and developing of discrete control systems. M. – 1962 State scientific & technical publish house of manufacturing literature. p. 684. (In Russian)

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