

# Multiprocessor System on Chip based on programmable processor cores Nios II Altera

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**Abstract – The features of a standard design flow facilities SOPC Builder Altera to develop multiprocessor systems are considered. Modeling and research of programmable multiprocessor cores NIOS II Altera, which are designed for high-performance control functions are completed.**

Key words – Multiprocessor System on Chip, System on a Programmable Chip Builder, Field-Programmable Gate Array, processor cores Nios II Altera, design flow, Cyclone II.

## I. Introduction

Multiprocessor systems-on-chip (MPSoC, Multiprocessor System on Chip) belong to a class of programmable embedded multiprocessor systems (IPS) and led the latest trends in digital embedded electronic systems. A wide range of tasks such as maintenance of networks, multimedia, management can achieve a significant increase in performance from the use of this class. Effective application, which is aimed at research in this paper is of real-time control as complex technological processes and diverse modern equipment: on-board systems, radars, satellite systems, robotics, biological systems, and so on.

Programmable technology facilitates rapid prototyping of electronic systems and allows you to explore new architectures and technologies without the problems associated with the implementation of electronic devices for custom integrated circuits ASIC (Application-specific Integrated Circuit) [2]. Leading companies offering application developers FPGA programmable processor cores specially designed for use in FPGA hardware and processor cores also equipped with built-in FPGA block RAM, peripheral circuits and communication.

## II. Problems of using Design Flow methodology

One of the most common methodologies for the development of embedded multiprocessor systems based on FPGA design has a hand (Hand-Tuned Design - manually customizable design), the use of unified (standard) thread design (Design Flow), which is offered by FPGA manufacturers with their CAD [2].

The two most well-known companies offering products EDK (Embedded Development Kit) from the company Xilinx [3] and SOPC Builder (System on a Programmable Chip Builder) Company's Altera [4]. The main benefits of the design flow are ease of specialized tools and availability

of libraries of standardized modules, as suppliers of software and hardware, and third-party manufacturers.

One of the problems of manual application design that is difficult to investigate and improve the entire space project completely to get the best possible architecture for a particular problem. This method can be a good choice for building small systems, where it is known as it should be designed architecture.

Another major problem is that the application flow design companies FPGA manufacturers cannot implement all the necessary designing multiprocessor systems for increasing their productivity and adaptation to classes solvable problems, including "on the fly" [1]. That standard design flow limits in the first place such an important advantage of FPGAs as flexibility of design. The functionality of design automation offered by library modules, programmable processor cores, interfaces advance due FPGA manufacturers, besides tools for flow design originally created for developing systems with one core, and have a number of disadvantages when it comes to high-performance multiprocessor systems. These issues are addressed in detail in [1], where the basis of a comprehensive analysis of the literature put forward the most important drawbacks standard design flows.

## III. Structural and software development in the Quartus II CAD and testing multiprocessor system

To implement the system educational and research stand DE2 (DE2 Development and Education Board) is used [6] with embedded FPGA Cyclone II EP2C35F672C6 Altera [6], which contains 33,216 logic elements on the chip. The total amount of internal memory (On-Chip Memory) chip is at 483,840 bits, which is about 59Kb. The stand built DE2 external to the FPGA chip memory - 8MB SDRAM, 512K SRAM, 1MB Flash Memory and other devices and interfaces [5].

Multiprocessor programmable core such as Nios II / s (small core size) are used [6]. Processor core contains a small number of logic elements in the crystal, compared to the more advanced version of Nios II / f, namely to 1,400 LEs, which is only 4% of the total area of the crystal FPGA Cyclone II; provides high performance 0, 74 DMIPS / MHz, at a frequency of core 165MHz, maximum performance will be 127 DMIPS.

SOPC Builder allows adding up to 60 processor cores of different shapes, but the number of processor cores is limited to the physical characteristics of the crystal, including its logical resources. For example chip is selected to implement the system Cyclone II EP2C35F672C6, can place up to 47 cores economical Nios II / e (economy core), in which no cash and giving performance to 31DMIPS, at a frequency of 200MHz. At the same time, this chip can hold up to 18 fast cores Nios II / f (Fast core), in which there are instruction cache and data cache, and performance is 218DMIPS at a frequency of 185MHz, which together with the use of parallel software can up to 3924 DMIPS.

A multiprocessor system contains 3 processor cores with instruction cache 4Kb, although the maximum amount of memory instructions in the kernel can be up to 64KB, but in this project we limited amount of internal memory chip. Each core is connected with an interval timer with a period of 1ms.

A multiprocessor system on chip occupies 32% of logic resource, namely 10,785 logic elements, and uses 46% of internal memory and is about 27Kb.

After synthesis of multiprocessor system in SOPC Builder structural module connects to the input and output circuit contacts (Fig. 1).

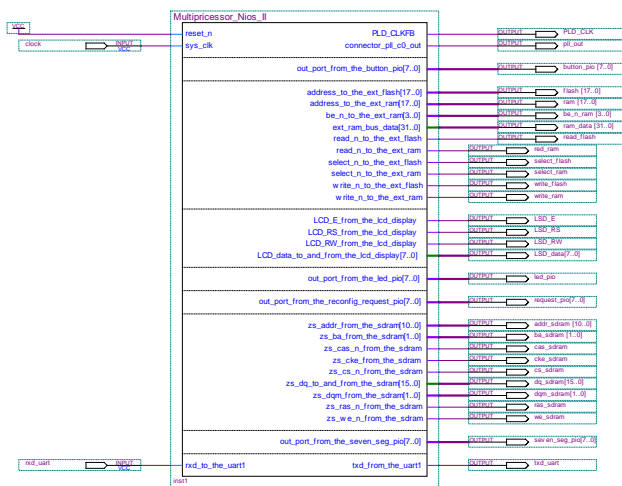


Fig. 1. Structural module in Quartus II CAD

Software environment Nios II Software Build Tools for Eclipse is using for initialization and programming processor cores. Test results can be previewed in the console window Nios II Software Build Tools for Eclipse (Fig. 2).

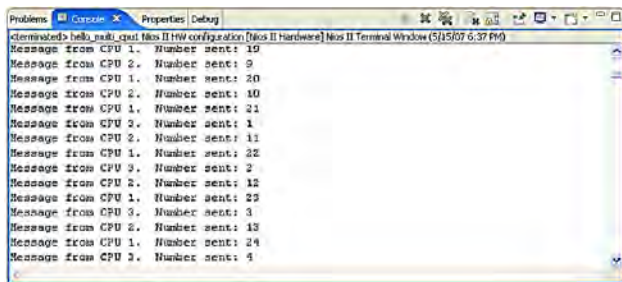


Fig. 2. Output of microprocessor system

## Conclusion

Embedded systems require the multiprocessor architecture for high performance computing, use-reduction capacity, physical size and cost. The use of programmable logic integrated circuits has greatly increased the speed of digital devices carried on a single chip.

In multiprocessor systems of this class software implementation distribution problems is only possible with

centralized management based on existing technologies parallel programming. Current and very promising task in the design of multiprocessor systems - automation of the distribution of tasks and output on the ability of dynamic reconfiguration is also disabled if the system limits the flow of design and architecture of the offered strictly

In the context of the above, it should be noted that the standard design tools are available for a wide range of developers, but they have some limitations in terms of speed and flexibility created systems design and effective for simple designing high performance systems.

The main focus of research in the design of high-performance multiprocessor systems based on FPGAs are overcoming these deficiencies and problems through the implementation of new methods for improving the efficiency of multiprocessor systems and creation on their basis of specialized tools that allow a more efficient architecture of FPGA-MPSoC.

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