CMOS Image Sensor on Microcavities and Local SOI-Structures

Anatolij Druzhinin, Victor Holota, Igor Kogut, Victor Dovgyj, Yuriy Khoverko

Abstract – **the structure of sensor images on "silicon-on-insulator" local structures is proposed and possibility of monolithic integration of sensing elements and signal processing systems is shown.**

Keywords – **image sensor, sensor element, SOI-structure, microcavities, monolithic integration.**

I. INTRODUCTION

Over the last decade CMOS image sensors high introduced in various fields of science and technology (optical metrology, astronomy, machine vision systems, mobile phones, digital cameras). Introduction of additional operations in standard CMOS processes allowed creating silicon image sensors, whose functional characteristics are not inferior, and sometimes prevailing image sensor based on charge-coupled devices. The most common architecture of silicon CMOS image sensor is CMOS monolithic and CMOS hybrid [1, 2]. In the monolithic architecture the photosensitive elements are built in integrated readout and signal processing circuits, and in the hybrid – are placed on a separate layer. One of the image sensors advantages is the possibility of monolithic integration on a single crystal in the form of "Image System on Chip" circuits that implement all the functions from reading signals to obtain images [3]. Functional characteristics of image sensors strongly depend on the geometry and topology of pixels and the impact of signals reading, amplification and digitization circuits. Therefore, in terms of integration of photosensitive elements with signal processing circuits and improves their functional characteristics with full dielectric isolation of circuit elements on a substrate, and another, more promising are the local SOI-structures [4].

The paper describes the sensor architecture with integrated image signal processing circuits that are implemented at local SOI-structures.

II. STRUCTURE OF THE IMAGE SENSOR

Structure of the image sensor was developed based on a monolithic architecture. The prototype of the CMOS pixel (discrete photosensitive cell that collects electrons generated by photons and converts the resulting charge in voltage) is an active pixel 3T APS [5]. The structure of the three transistors pixel is shown in Fig 1.

Pixels with three transistors are used mainly in conventional devices. In the devices for scientific applications with higher requirements for sensitivity, quantum efficiency, dynamic range, time integration charge, dark current, are used pixels with four, five and six transistors.

The surface of the photodiodes is flat and covered with thin-film materials that reduce reflection and enhance transmission rate of incident light. For a color image on the surface of photodiodes placed red, blue or green light filter, and above which is set the optical focusing microlenses. The main element that defines the functional characteristics of the pixel is photosensitive element. Therefore, all the structural elements that are placed on the surface of photodiodes impair its functional characteristics.

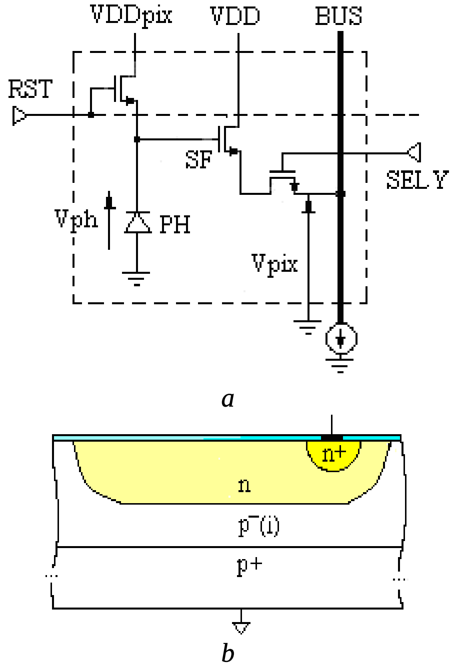

Fig. 1 The structure of the active pixel with three transistors: *a*) PH – photodiode, RST – signal of photodiode reverse bias, SF – transistor to convert the charge to voltage, SELY – voltage readout signal, BUS – readout bus, б) *n* – diffusion of *n*-type conductivity, p^- *(i)* – epitaxial layer of *p*-type conductivity, p+ – silicon substrate

In this paper original structure as photosensitive element and the transistor control circuit are proposed. This structure has a smaller number of structural elements and the control circuit dielectrically isolated from the photosensitive element, Fig. 2.

Initially ***p-i-n*** diode is formed by standard technology for such a structure. Epitaxial layer of p^--type (*i*-area), increases the depleted area width of inversely biased junction. Photonic electrons that fall into this area, captured by the electric field and accumulated in the *n*-diffusion area. At the next technological stage in *n*-diffusion layer formed simultaneously partially and completely buried microcavity

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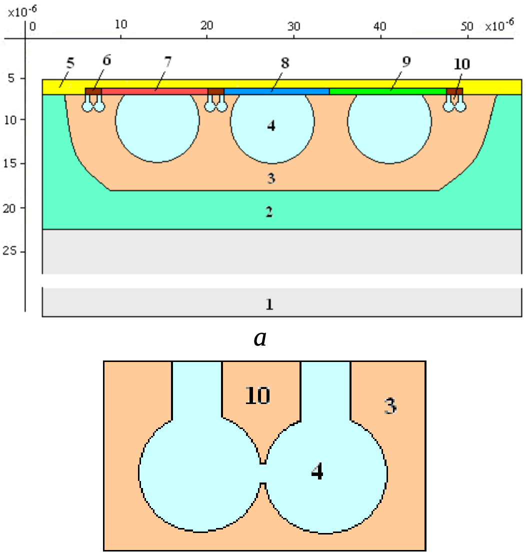
Anatolij Dryzhinin, Lviv Polytechnik National University, Bandery Str., 12, Lviv, 79046, UKRAINE,
E-mail:druzh@polynet.lviv.ua
Victor Holota, Igor Kogut, Victor Dovgyj, V. Stefanyk Precarpathian National University, Shevchenka Str., 57, Ivano-Frankivsk, 76025, UKRAINE, E-mail:kre@pu.if.ua
Yuriy Khoverko, International laboratory of high magnetic fields and low temperatures, Gajowicka St., 53-421 Wroclaw, Poland

by original technology [6]. The inner surface partially depth cavities of large diameter are photosensitive elements. Fully deep cavities on the order of smaller diameter forming local SOI-structures, on which MOS transistors control circuits are created. Cavities filled with pyrolytic deposited silicon oxide. In large cavities silicon oxide are optical microlenses, and in small cavities – insulating layers of local SOI-structures. Cylindrical cavities increases the area of photosensitive area 3.3 times, compared with a flat area at the corner cut off the central segment of 90°. This form also improves the absorption of light with repeated reflection. The variable width of the depletion region in the inversely biased photodiodes increases the number of generated electrons for different wavelengths of light. Area of photosensitive element is the main parameter which determines the value of the output signal. Increasing this parameter reduces the requirements for other parameters.



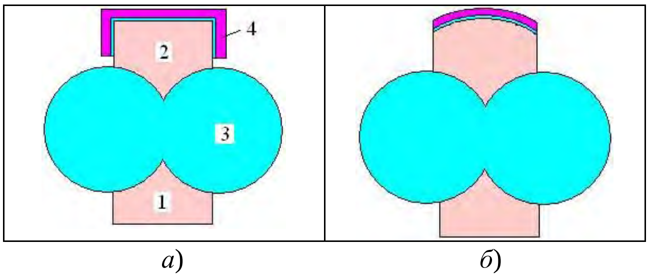
a

b

Fig.2. Structure of the photosensitive element of depth micro cavities: *a*) 1 – silicon substrates *p*+-type conductivity, 2 – epitaxial layer of *p*-type conductivity, 3– diffusion of *n*-type conductivity, 4 – silicon oxide, 5 – silicon nitride, 6 – polycrystalline silicon, 7, 8, 9 – red, blue and green filters, *b*) 10 – local SOI-structure

On the local SOI-structure can be a standard CMOS technology to form the dielectric isolated MOS-transistors control circuits. The advantage over standard local SOI-structures that can be placed in appropriate places, creating a SOI-layer of different thickness, and MOS transistors with rounded shape of gates, Fig. 3. At this gate form electric field is uniform across the width of the channel. Transistor has a higher switching speed when the gate has a rounded shape, not rectangular.

Control circuit transistors set time of integration charge, transform a charge in the voltage and put a signal in the output bus. The form of the integrator and the output signal and is shown in Fig. 4.



а)　　*б*)

Fig3. 3. CMOS SOI transistors: a) with rectangular shape of gate; б) with rounded shape of gate

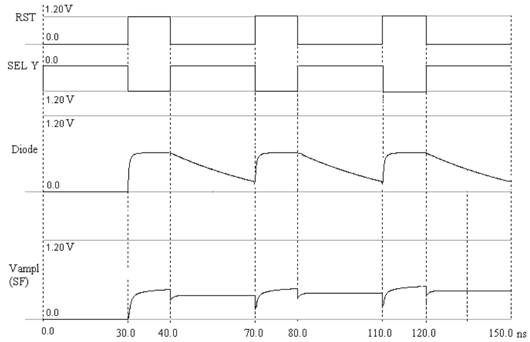


Fig.4. Timing samples

III. CONCLUSIONS

The structure of image sensor in which the sensing element is a inner surface of cavities, and the control circuit is placed on local SOI-structures is proposed. This structure enhances the image sensor quantum efficiency and reduces leakage currents of control circuits.

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